Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 1-3. These sheets, which include Figures 1-3, replace the original sheets including the same figures.

Attachment: Replacement Sheets

REMARKS

In the Office Action dated February 27, 2007, the Examiner acknowledged the election of the Group I claims 1-4, objected to the informality of the drawings, objected to the specification, and rejected claims 1-4 under 35 USC 102 as anticipated by Pederson in US Patent 6,066,960. In response thereto, the Applicant has amended the specification, submitted formal drawings, amended claim 1 and cancelled claim 5. Claims 1-4 remain at issue.

The Drawings

The Applicant has submitted a new set of formal drawings. It is requested that the objection to the drawings now be withdrawn.

The Specification

The Applicant has amended the Abstract to make it less than 150 words. Again, the Applicant requests that this objection be withdrawn.

The Art Rejection

The Examiner has rejected claims 1-4 as anticipated by Pederson. The Applicant strongly disagrees. Pederson does not anticipate the claims.

As correctly noted by the Examiner, Figure 1D of Pederson appears to be the most relevant. Pederson characterizes Figure 1D as a 16-bit adder where "*many single bit summations must occur.*" See column 2, lines 26-27. By single bit summations, Pederson means two bits are added together at each stage of the adder. This is clearly illustrated in Figure 1D. For example, the operands (a1, b1), (a2,b2) and (an,bn) are added in logic elements LE1, LE2 and LEn respectively. The so called "third" signal the Examiner is relying on in the rejection is not an operand at all, but the carry-in signal from the previous 2-bit adder.

In contrast, the claims of the present application are clear that each LUT logic cell receives (i) three input signals; and (ii) generate a sum and carry signal resulting from adding the three input signals. For the sake of clarity, the Applicant has amended the claim to make it clear that the LUT logic cell of the present invention adds three (or potentially more) operands, not two operands and a carry-in signal as taught in the prior art. Claim 1 is therefore not anticipated by Pederson.

Although patentable in their own right, claims 2-4 are also allowable based on their dependency on claim 1.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a

telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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